Translation

PATENT COOPERATION TREATY

PCT

INTERNATIONAL PRELIMINARY EXAMINATION REPORT

(PCT Article 36 and Rule 70)

Applicant's or agent's file reference 12626WO /mz	FOR FURTHER ACTION	See Notification of Transmittal of International Preliminary Examination Report (Form PCT/IPEA/416)
International application No. PCT/EP2003/009179	International filing date (*day/month/year*) 19 August 2003 (19.08.2003)	Priority date (*day/month/year*) 29 August 2002 (29.08.2002)
International Patent Classification (IPC) or national classification and IPC G06F 17/50		
Applicant INFINEON TECHNOLOGIES AG		

1. This international preliminary examination report has been prepared by this International Preliminary Examining Authority and is transmitted to the applicant according to Article 36.

2. This REPORT consists of a total of 5 sheets, including this cover sheet.

   ☒ This report is also accompanied by ANNEXES, i.e., sheets of the description, claims and/or drawings which have been amended and are the basis for this report and/or sheets containing rectifications made before this Authority (see Rule 70.16 and Section 607 of the Administrative Instructions under the PCT).

   These annexes consist of a total of 5 sheets.

3. This report contains indications relating to the following items:

   - I ☒ Basis of the report
   - II ☐ Priority
   - III ☐ Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
   - IV ☐ Lack of unity of invention
   - V ☒ Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement
   - VI ☐ Certain documents cited
   - VII ☐ Certain defects in the international application
   - VIII ☐ Certain observations on the international application

Date of submission of the demand 15 March 2004 (15.03.2004)	Date of completion of this report 02 August 2004 (02.08.2004)
Name and mailing address of the IPEA/EP Facsimile No.	Authorized officer Telephone No.

INTERNATIONAL PRELIMINARY EXAMINATION REPORT

International application No.
PCT/EP2003/009179

I. Basis of the report

1. With regard to the elements of the international application:*

☐ the international application as originally filed

☒ the description:

pages 1-17, as originally filed

pages _____, filed with the demand

pages _____, filed with the letter of _____

☒ the claims:

pages _____, as originally filed

pages _____, as amended (together with any statement under Article 19

pages _____, filed with the demand

pages 1-16, filed with the letter of 14 July 2004 (14.07.2004)

☒ the drawings:

pages 1, as originally filed

pages _____, filed with the demand

pages _____, filed with the letter of _____

☐ the sequence listing part of the description:

pages _____, as originally filed

pages _____, filed with the demand

pages _____, filed with the letter of _____

2. With regard to the language, all the elements marked above were available or furnished to this Authority in the language in which the international application was filed, unless otherwise indicated under this item.
These elements were available or furnished to this Authority in the following language _____ which is:

☐ the language of a translation furnished for the purposes of international search (under Rule 23.1(b)).

☐ the language of publication of the international application (under Rule 48.3(b)).

☐ the language of the translation furnished for the purposes of international preliminary examination (under Rule 55.2 and/or 55.3).

3. With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, the international preliminary examination was carried out on the basis of the sequence listing:

☐ contained in the international application in written form.

☐ filed together with the international application in computer readable form.

☐ furnished subsequently to this Authority in written form.

☐ furnished subsequently to this Authority in computer readable form.

☐ The statement that the subsequently furnished written sequence listing does not go beyond the disclosure in the international application as filed has been furnished.

☐ The statement that the information recorded in computer readable form is identical to the written sequence listing has been furnished.

4. ☐ The amendments have resulted in the cancellation of:

☐ the description, pages _____

☐ the claims, Nos. _____

☐ the drawings, sheets/fig _____

5. ☐ This report has been established as if (some of) the amendments had not been made, since they have been considered to go beyond the disclosure as filed, as indicated in the Supplemental Box (Rule 70.2(c)).**

* *Replacement sheets which have been furnished to the receiving Office in response to an invitation under Article 14 are referred to in this report as "originally filed" and are not annexed to this report since they do not contain amendments (Rule 70.16 and 70.17).*

** *Any replacement sheet containing such amendments must be referred to under item 1 and annexed to this report.*

V. Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1. Statement

Novelty (N)	Claims	1-16	YES
	Claims		NO
Inventive step (IS)	Claims	1-16	YES
	Claims		NO
Industrial applicability (IA)	Claims	1-16	YES
	Claims		NO

2. Citations and explanations

1. The closest prior art is described in document XP002270149. The incorporation into a verification module of various predefined architectural variants for multipliers, and the comparison of all these variants with the synthesised circuit, is regarded in that document as unpromising. A Boolean mapping algorithm is used instead, which extracts a net of half adders from a gate network list of an adding circuit. An equivalence test of the adding circuit is then carried out by a known arithmetic representation on the binary plane. This method is limited to isolated individual multiplication functions.

2. Disadvantages of the prior art: in practice, once synthesised circuits are optimised, the multiplier gates will be intertwined with other gates. For the method to remain feasible, additional information on the multiplier structure is required.

3. Technical problem: the following technical problem is therefore addressed: to efficiently verify digital circuits by equivalence testing, in the absence of explicit information on the

implementation alternatives of the circuit and without limiting the verification to a specific implementation alternative.

2. **Solution according to the present invention**

The present invention solves the problem of the absence of additional information on the implementation alternative used by selecting, among all possible implementation alternatives, those having the highest degree of structural concordance with the synthesised circuit for verification purposes. In order to determine those alternatives, each implementation alternative is simulated in combination with the reference description and compared with a simulation of the circuit. The implementation alternative having the largest number of computation points in common with the circuit in a plurality of simulation patterns is chosen (heuristic approach). The prior art does not hint at this solution (and D1 advises against it). Consequently, the subject matter of claim 1 is not obvious to a person skilled in the art.